

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A pipelined data processor operating
2 in a plurality of pipeline phases including at least an instruction
3 decode pipeline phase and an execution pipeline phase capable of
4 predicated instruction execution dependent upon the state of an
5 instruction designated predicate register comprising:

6 a data register file including a plurality of read/write,
7 general purpose data registers;

8 an instruction decode unit operative during an instruction
9 decode pipeline phase receiving fetched instructions and
10 determining the identity of at least one source operand data
11 register, a destination operand data register and one of a
12 plurality of functional units for execution of each instruction,
13 said instruction decode unit further identifying a predicate
14 register responsive to receipt of a predicated instruction;

15 a said plurality of functional units operative during an
16 execution pipeline phase connected to said instruction decode unit
17 for performing a data processing operation on at least one source
18 operand recalled from at least one corresponding instruction
19 designated source data register and producing a result, said
20 functional unit responsive to a predicate instruction to write said
21 result to an instruction designated destination data register if
22 said corresponding predicate data register has a first state and to
23 nullify said instruction and not write said result if said
24 predicate register has a second state opposite to said first state;

25 a scoreboard bit corresponding to each data register capable
26 of serving as a predicate register, each scoreboard bit connected
27 to said instruction decode unit to be set to a first digital state
28 upon determining said corresponding data register is a destination

29 for an instruction and connected to said plurality of functional
30 units to be reset to a second digital state opposite to said first
31 digital state upon functional unit write of a result to said
32 corresponding data register; and

33 each functional unit is further operative responsive to a
34 predicate instruction during ~~a~~ said instruction decode pipeline
35 phase to nullify said predicate instruction of a following
36 execution phase by operating at a reduced power state relative to
37 normal instruction operation if said predicate register has said
38 second state and said corresponding scoreboard bit has said second
39 state.

1 2. (Original) The pipelined data processor of claim 1,
2 wherein:

3 said functional unit is further operative to reset said
4 scoreboard bit to said second digital state upon nullification of
5 said instruction designating a corresponding data register as a
6 destination operand data register.

3. (Canceled)

1 4. (Currently Amended) A method of operating a pipelined
2 data processor operating in a plurality of pipeline phases
3 including at least an instruction decode pipeline phase and an
4 execution pipeline phase capable of predicated instruction
5 execution dependent upon the state of an instruction designated
6 predicate register comprising the steps of:

7 setting a scoreboard bit to a first digital state upon
8 determining a corresponding data register is a destination for an
9 instruction;

10 resetting a scoreboard bit to a second digital state opposite
11 to said first digital state upon a write of a result to said
12 corresponding data register;
13 performing a data processing operation via a corresponding
14 functional unit on at least one source operand recalled from at
15 least one corresponding instruction designated source data register
16 and producing a result in response to a predicate instruction
17 designating a corresponding predicate data register and writing
18 said result to an instruction designated destination data register
19 if said corresponding predicate data register has a first state;
20 nullifying a predicate instruction ~~and~~ by not writing said
21 result to the instruction designated destination data register via
22 said corresponding functional unit if said corresponding predicate
23 register has a second state opposite to said first state; and
24 nullifying a predicate instruction for a following execution
25 phase by operating said corresponding functional unit at a reduced
26 power state relative to normal instruction operation if said
27 corresponding predicate register has said second state and said
28 corresponding scoreboard bit has said second state during a prior
29 decode phase.

1 5. (Original) The method of claim 4, further comprising the
2 step of:

3 resetting a scoreboard bit to a second digital state upon
4 nullification of said instruction designating said corresponding
5 data register as a destination operand data register.

6. (Canceled)

1 7. (Currently Amended) The method of claim 4 further
2 comprising the ~~step~~ steps of:

3 statically scheduling instruction execution via a compiler;
4 and
5 scheduling via said compiler a last write to a data register a
6 ~~predetermined number of pipeline phases before an execution a~~
7 decode phase of a predicate instruction designating said data
8 register as a predicate register.

1 8. (New) The pipelined data processor of claim 1, wherein:
2 each functional unit is operable at said reduced power state
3 by not fetching at least one instruction operand and not toggling a
4 corresponding register read port during said following execution
5 phase.

1 9. (New) the pipelined data processor of claim 1, wherein:
2 each functional unit is operable at said reduced power state
3 by not powering said functional unit during said following
4 execution phase.

1 10. (New) The method of claim 4, wherein:
2 said step of operating said corresponding functional unit at a
3 reduced power state includes not fetching at least one instruction
4 operand and not toggling a correspond register read port during
5 said following execution phase.

1 11. (New) The method of claim 4, wherein:
2 said step of operating said corresponding functional unit at a
3 reduced power state relative includes not powering said functional
4 unit during said following execution phase.